WHAT IS CLAIMED IS

1. A semiconductor device, comprising:

a mount substrate;

a high-frequency transmission line provided on a top surface of said mount substrate;

a semiconductor chip mounted on said top surface of said mount substrate in a facedown state in electrical contact with said high-frequency transmission line, said semiconductor chip thereby having a bottom surface facing said top surface of said mount substrate; and

a depression formed on said top surface of said mount substrate.

2. A semiconductor device as claimed in claim 1, wherein said semiconductor chip carries a projection on said bottom surface, said semiconductor chip being mounted on said top surface of said mount substrate such

that said projection is accepted into said depression, and wherein said depression has a depth set such that said projection does not contact a surface of said depression.

3. A semiconductor device as claimed in claim 2, further comprising an interconnection structure on said high-frequency transmission line, said semiconductor chip being connected electrically and mechanically to said high-frequency transmission line via said interconnection structure, wherein said depth of said depression is set such that said depth is equal to or larger than a height of said projection from which a height of said interconnection structure is subtracted.

4. A semiconductor device as claimed in claim 3, wherein said interconnection structure includes a solder bump.

5. A semiconductor device as claimed in claim 2, wherein said semiconductor chip carries a coplanar transmission line on said bottom surface thereof, and wherein said projection is an air bridge structure forming a part of said coplanar transmission line.

6. A semiconductor device as claimed in claim 1, wherein said depression forms a through-hole penetrating through said mount substrate from said top surface to a bottom surface opposite to said top surface.

7. A semiconductor device as claimed in claim 1, wherein said high-frequency transmission line is a microstrip line including a ground layer, a dielectric layer provided on said ground layer and a wiring layer provided on said dielectric layer.

8. A semiconductor device as claimed in claim 7, wherein said dielectric layer is formed of SiO_2.

9. A semiconductor device as claimed in claim 7, wherein said dielectric layer is formed of polyimide.

10. A semiconductor device as claimed in claim 1, wherein said substrate is formed of Si.

11. A semiconductor device as claimed in claim 1, wherein said substrate is formed of polyimide.

12. A semiconductor device as claimed in

claim 1, wherein said depression is defined by a crystal surface.

13. A method of fabricating a semiconductor device comprising a mount substrate; a high-frequency transmission line provided on a top surface of said mount substrate; a semiconductor chip mounted on said top surface of said mount substrate in a facedown state in electrical contact with said high-frequency transmission line, said semiconductor chip thereby having a bottom surface facing said top surface of said mount substrate; and a depression formed on said top surface of said mount substrate, said semiconductor chip carrying an air bridge structure on said bottom surface, said method comprising a steps of:

forming said depression by an etching process to said top surface of said mount substrate; and

mounting said semiconductor chip on said mount substrate such that said air bridge structure is accommodated into said depression.

14. A method as claimed in claim 13, wherein said mount substrate is formed of Si, and wherein said etching step includes an anisotropic wet etching process applied to said top surface of said mount substrate.

15. A method as claimed in claim 13, wherein said mount substrate is formed of polyimide, and wherein said etching step includes a dry etching process applied to said top surface of said mount substrate.